Electrodeposited Mn-Co Alloy Coating For SOFC Interconnects

H.A. McCrabb[1], B. Kagajwala[1] T.D. Hall[1], H. Zhang[2], X. Liu[2], S. Snyder[1] E.J. Taylor[1]

[1]Faraday Technology Inc., 315 Huls Dr., Clayton, OH 45315, USA

[2]West Virginia University,Dept. of Mechanical and Aerospace Eng.ESB, Morgantown, WV, 26506, USA

Overall Objective

Develop, optimize & validate an inexpensive manufacturing process for coating metallic SOFC interconnects with Co and Mn.

Introduction

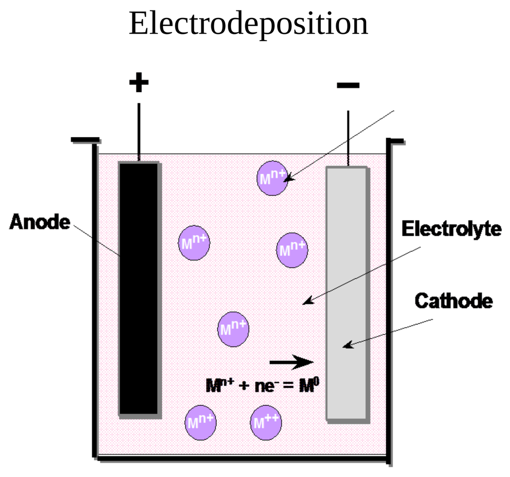
Reducing SOFC operating temperatures below 1000 ºC has permitted less resistive and expensive ferritic stainless steel interconnects to replace ceramic materials. However, even specially developed ferritic alloys operated at elevated temperatures for lengthy periods of time form a chromia scale that increases the interconnect resistance and results in chrome diffusion from the interconnect to the cathode that causes a reduction in cathode performance. One attractive method to resolve the chromia scale growth and diffusion issues is to electrodeposit a Mn-Co alloy coating onto the interconnect surface and subsequently convert it to a $(Mn,Co)_3O_4$ spinel.

Under funding from the Department of Energy, Faraday Technology and WVU are developing, optimizing and validating an electrodeposition process to apply high-quality coatings to SOFC interconnects in a mass production scenario. The FARADAYIC℠ Electrodeposition Process can be used to deposit a Mn-Co alloy with a controlled composition and thickness that can subsequently be converted to a spinel by thermal exposure at high temperatures in an oxidizing environment. Faraday has scaled its process capabilities from 25 cm^2 to 100 cm^2 SOFC interconnects and demonstrated the ability to coat interconnects containing gas flow field features. Continued analysis and refinement of the economic assessment based on using batch manufacturing for the pulse reverse electrodeposition process demonstrated that the innovative coating technology can meet DOE's high volume target of 1.6 million plates per annum for 250 MW fuel cell stacks at a cost of ~$1.85 per 625 cm^2 coated interconnect.

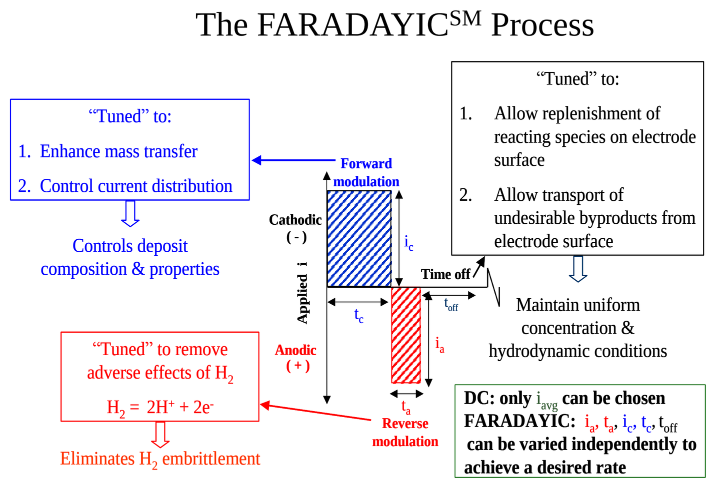
Approach

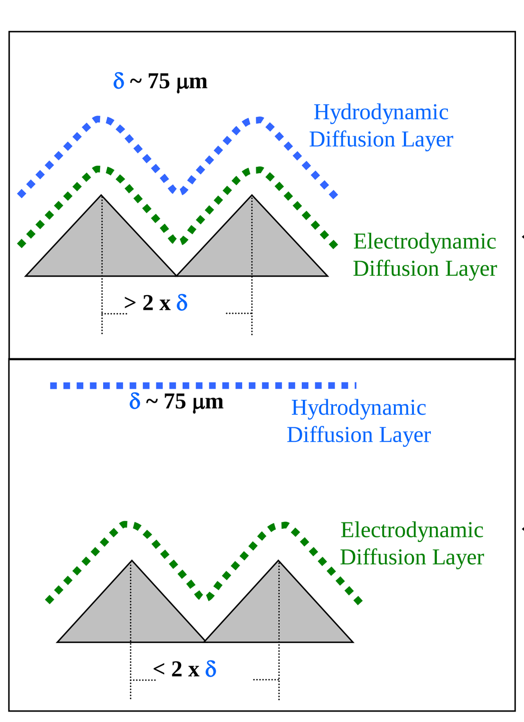
The FARADAYIC℠ Electrodeposition Process

Electrodeposition



The FARADAYIC℠ Process





The appropriate waveform can alter the thickness of the pulsating diffusion layer and effectively focus or defocus the current distribution to create non-uniform or uniform deposition respectively.

← Macroprofile: Diffusion layer tends to follow the surface contour. Mass transport control results in a uniform current distribution or a conformal deposit during deposition.

← Microprofile: Diffusion layer thickness surface roughness. Mass transport control results in a non-uniform current distribution.

The FARADAYIC℠ Electrodeposition process…

- Enables alloy composition control
- Enables control of coating uniformity for flow field patterns
- Maintains fast processing times to enable high throughput manufacturing
- Is an inexpensive manufacturing process for SOFC interconnect coatings

Milestones

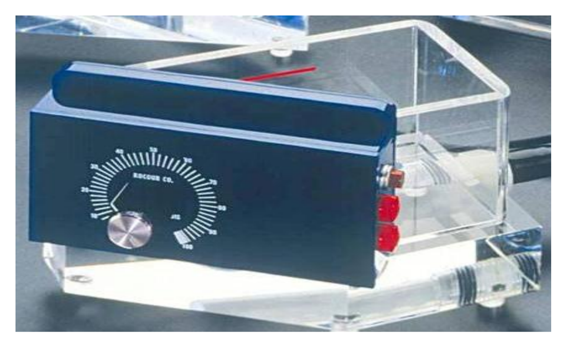
Fiscal Year	*Title*	*Planned Completion*	*Percent Complete*
2011	1. Design/modification of 10" x 10" electrodeposition cell	May 2011	100%
2012	2. Long-term high temperature, thermal evaluation	August 2012	70%
2012	3. Process development for 4"x4" planar interconnects	May 2012	100%
2012	4. Process development for 4"x4" pattern interconnects	June 2012	10%
2012	5. Long-term on-cell performance evaluation	August 2012	10%
2012	6. Qualification/demonstration of IC in single cell test rig	September 2012	0%

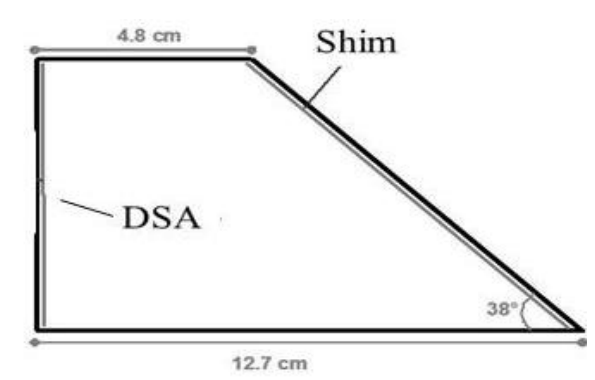
Previous Accomplishments

Hull Cell Experiments to Determine Coating Composition Possibilities

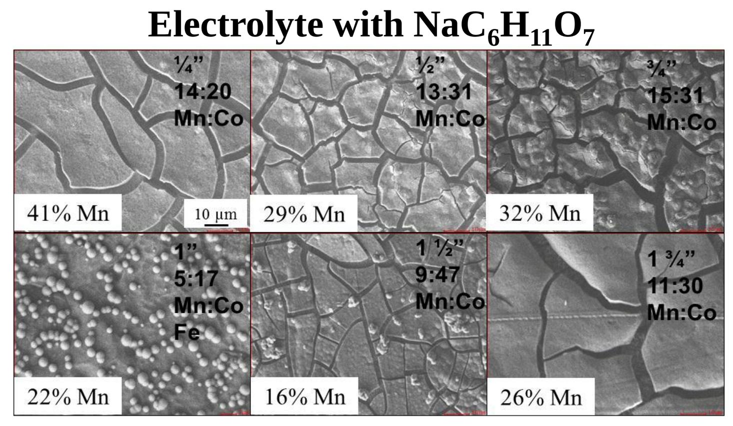
Enables investigation into the effect of various parameters on deposit properties during a single experiment

- Current density
- Temperature
- Electrolyte composition
- Additives

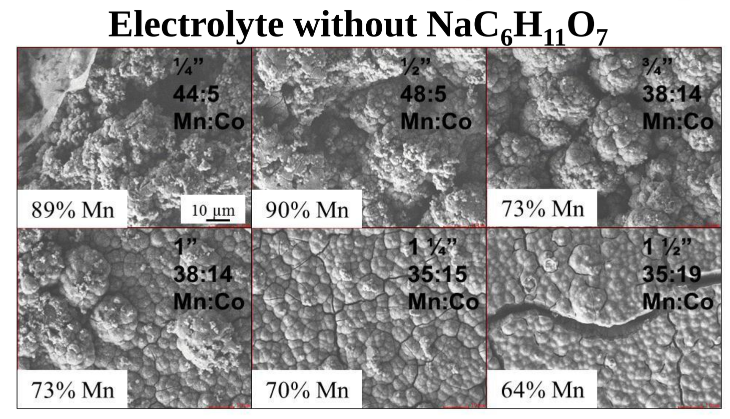




Electrolyte with $NaC_6H_{11}O_7$



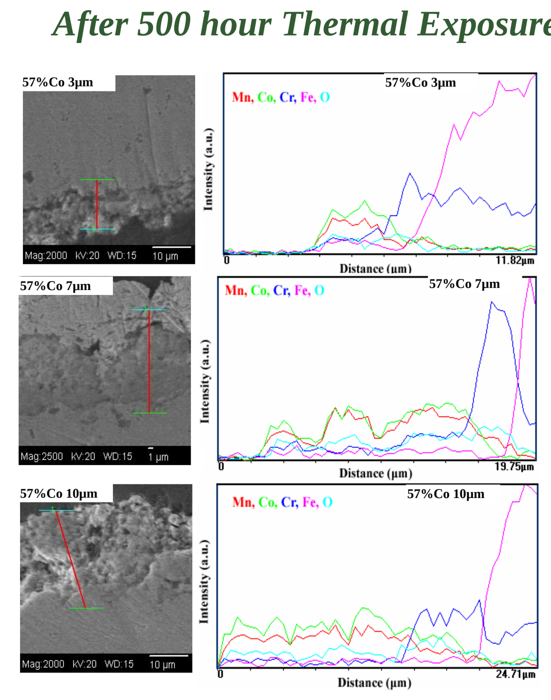
Electrolyte without $NaC_6H_{11}O_7$



Electrolyte without $NaC_6H_{11}O_7$ was selected for Phase I work on 5 cm x 5 cm T441 planar substrates because at reasonable current densities and metal ion concentrations results suggested

- Potential for higher Mn content in coating
- Less microcracking
- Higher current efficiency
  - Faster coating deposition rates

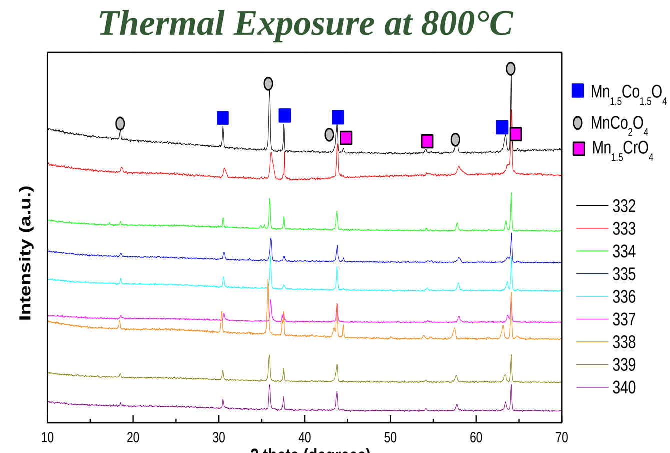
Coating Microstructure and Composition After 500 hour Thermal Exposure



ASR at 800°C

mΩ cm^2	100 hr	200 hr	500 hr
3 µm 40% Co	35	57	49
7 µm 40% Co	62	7	32
10 µm 40% Co	22	-	36
3 µm 85% Co	31	75	20
7 µm 85% Co	59	40	54
10 µm 85% Co	37	23	22
3 µm 57% Co	-	34	26
7 µm 57% Co	-	-	12
10 µm 57% Co	-	-	12

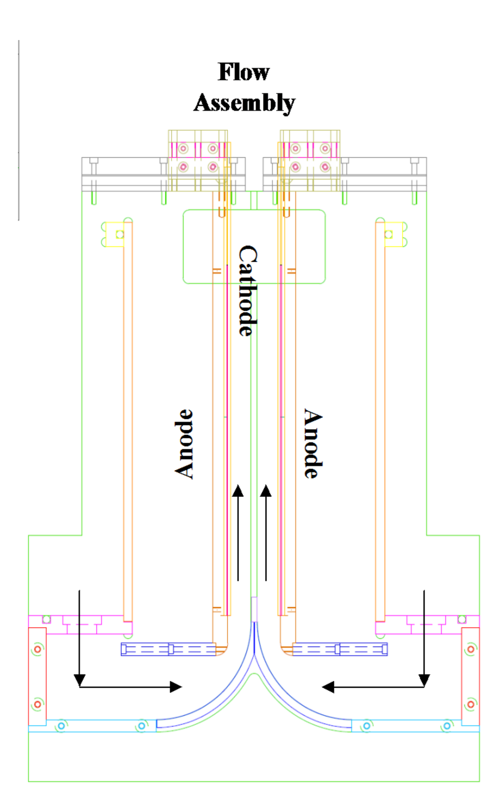
Crystal Structure After 500 hour Thermal Exposure at 800°C



Processing Equipment

Electrochemical Cell

Based upon Faraday's electrochemical cell design that facilitates uniform flow across the surface of a flat substrate (US patent #7,553,401)



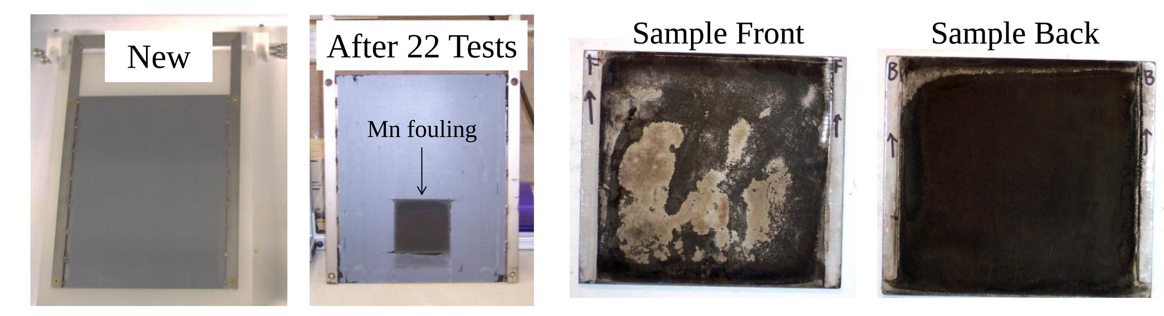
Modified FARADAYIC℠ Electrodeposition Cell for coating patterned interconnect substrates ranging in size from 6.5 cm^2 to 625 cm^2

Results

Process Scale-up from 25 cm^2 to 100 cm^2

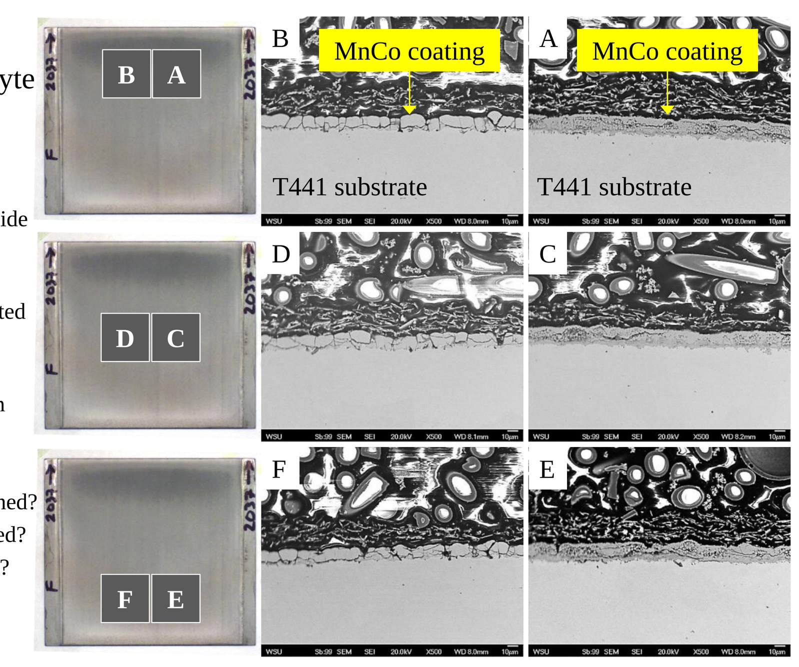
Challenges encountered during scale up from 25 cm^2 to 100 cm^2

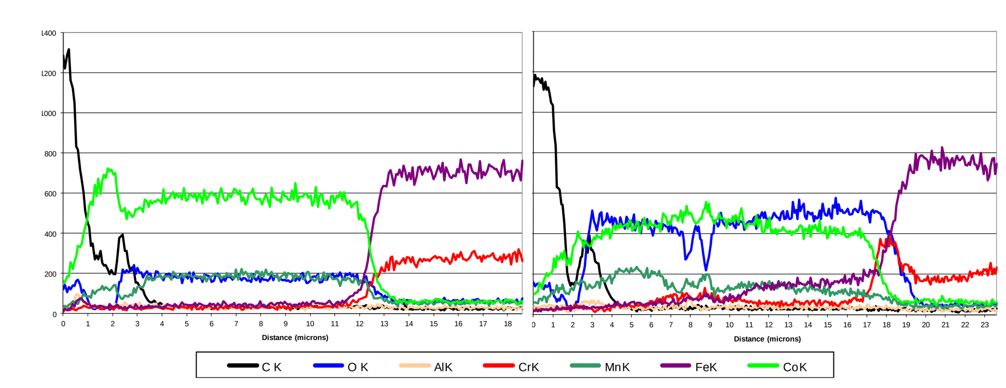
- Anode fouling
- Adhesion
- Process repeatability



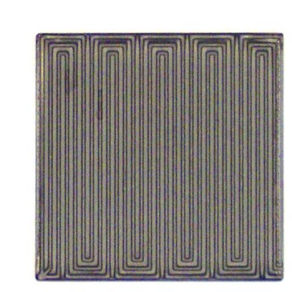
Solution: Revisit plating electrolyte with $NaC_6H_{11}O_7$

- Addition of $NaC_6H_{11}O_7$ to electrolyte
  - Observed benefits
    - Boric acid dissolves completely
    - Improved buffer capacity
    - Complexing metal ions prevents hydroxide formation
    - Anode fouling doesn't occur
    - Improved coating adhesion in as-deposited state
    - Coating deposition rate appears linear
    - Coating thickness doesn't decrease upon spinel conversion
  - Associated challenges
    - Can a high enough Mn content be obtained?
    - Can the microcracking issue be addressed?
    - Is the coating deposition rate acceptable?
    - Is the process repeatability improved?

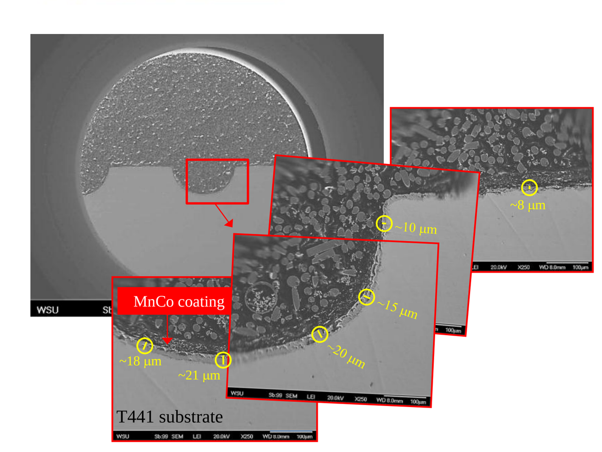


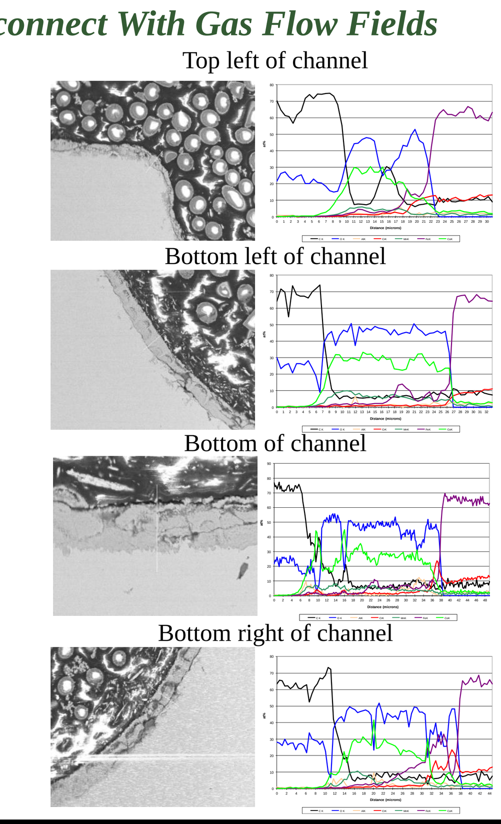


25 cm^2 430 Stainless Steel Interconnect With Gas Flow Fields



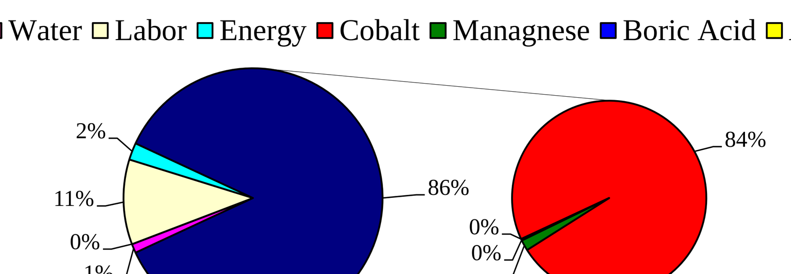
- 3 channel serpentine pattern
- Channel width ~ 0.9 mm
- Rib width ~ 0.8 mm
- Channel depth ~ 0.45 mm





Economic Analysis

Current cost analysis of coating process based upon batch manufacturing of 1,600,000 plates per annum at a cost of ~$1.85 per 625 cm^2 coated interconnect.



Accomplishments/Future Work

FY 2012 Accomplishments

- Continued optimization of FARADAYIC℠ Electrodeposition Process parameters in order to optimize coating thickness, coating composition and coating adhesion
- Improved coating uniformity across T441 planar interconnects at the 100 cm^2 scale
- Demonstrated coating process for 25 cm^2 430 stainless steel interconnect containing gas flow fields
- Continued refinement of economic analysis to assess economic viability of FARADAYIC℠ Electrodeposition Process for high volume batch manufacturing

Future Work

- Development, optimization and validation of the FARADAYIC℠ Electrodeposition Process for 100 cm^2 interconnects with gas flow field features
- Long-term on-cell performance evaluation of button cells
- Qualification/Demonstration of Interconnect Coating in Single Cell Test Rig under ideal SOFC operating conditions by potential commercial partners
- Continued development of a more comprehensive economic assessment of the electrodeposition coating process as it relates to interconnect manufacturing.

Acknowledgements

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Principal Investigator: Heather McCrabb, Company Name: Faraday Technology, Inc., Address: 315 Huls Drive, Clayton, OH 45315, Phone: 937-836-7749, E-mail: heathermccrabb@faradaytechnology.com, Company website: faradaytechnology.com